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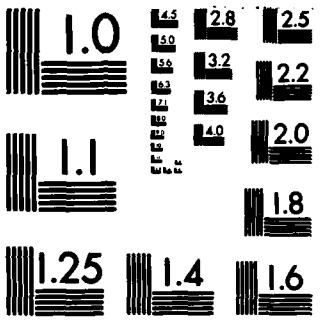


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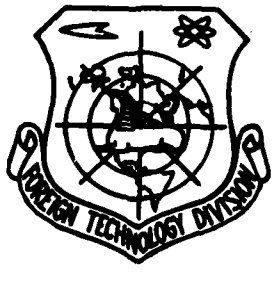
# FOREIGN TECHNOLOGY DIVISION


A TWO-CYCLE SHIFT REGISTER WITH ERROR DETECTION

by

R. E. Gut, V. B. Pogodin

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By: R. E. Gut, V. B. Pogodin

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PREPARED BY:

TRANSLATION DIVISION
FOREIGN TECHNOLOGY DIVISION
WP-AFB, OHIO.

## U. S. BOARD ON GEOGRAPHIC NAMES TRANSLITERATION SYSTEM

| Block | Italic | Transliteration | Block | Italic | Transliteration |
|---|---|---|---|---|---|
| А а | *А а* | A, a | Р р | *Р р* | R, r |
| Б б | *Б б* | B, b | С с | *С с* | S, s |
| В в | *В в* | V, v | Т т | *Т т* | T, t |
| Г г | *Г г* | G, g | У у | *У у* | U, u |
| Д д | *Д д* | D, d | Ф ф | *Ф ф* | F, f |
| Е е | *Е е* | Ye, ye; E, e* | Х х | *Х х* | Kh, kh |
| Ж ж | *Ж ж* | Zh, zh | Ц ц | *Ц ц* | Ts, ts |
| З з | *З з* | Z, z | Ч ч | *Ч ч* | Ch, ch |
| И и | *И и* | I, i | Ш ш | *Ш ш* | Sh, sh |
| Й й | *Й й* | Y, y | Щ щ | *Щ щ* | Shch, shch |
| К к | *К к* | K, k | Ъ ъ | *Ъ ъ* | " |
| Л л | *Л л* | L, l | Ы ы | *Ы ы* | Y, y |
| М м | *М м* | M, m | Ь ь | *Ь ь* | ' |
| Н н | *Н н* | N, n | Э э | *Э э* | E, e |
| О о | *О о* | O, o | Ю ю | *Ю ю* | Yu, yu |
| П п | *П п* | P, p | Я я | *Я я* | Ya, ya |

*ye initially, after vowels, and after ъ, ь; e elsewhere.
When written as ё in Russian, transliterate as yë or ë.

## RUSSIAN AND ENGLISH TRIGONOMETRIC FUNCTIONS

| Russian | English | Russian | English | Russian | English |
|---|---|---|---|---|---|
| sin | sin | sh | sinh | arc sh | $\sinh^{-1}$ |
| cos | cos | ch | cosh | arc ch | $\cosh^{-1}$ |
| tg | tan | th | tanh | arc th | $\tanh^{-1}$ |
| ctg | cot | cth | coth | arc cth | $\coth^{-1}$ |
| sec | sec | sch | sech | arc sch | $\operatorname{sech}^{-1}$ |
| cosec | csc | csch | csch | arc csch | $\operatorname{csch}^{-1}$ |

| Russian | English |
|---|---|
| rot | curl |
| lg | log |

## GRAPHICS DISCLAIMER

**All figures, graphics, tables, equations, etc. merged into this translation were extracted from the best quality copy available.**

# A TWO-CYCLE SHIFT REGISTER WITH ERROR DETECTION

R. E. Gut and V. B. Pogodin

The invention pertains to the area of computer technology. Single-cycle registers with error detection are known. However, in them the error detection block is suitable only for the class of single-cycle registers.

Also known are two-cycle shift registers in which the emergence of undetected errors is possible.

In the proposed two-cycle register, to increase the reliability of error detection the first outputs of the primary and auxiliary flip-flop of each digit are connected with the inputs of one element, "EXCLUSIVE-OR," the output of which is connected with input of the first element "OR," the second outputs of the main flip-flop of each digit and the auxiliary flip-flop of the following digit are connected with the inputs of each element "EXCLUSIVE-OR," the output of which is connected with the input of the second element "OR," the outputs of elements "OR," are connected with the input of the element "AND" which corresponds to it, the other input of which is connected with the output of the additional flip-flop, the inputs of which are connected with the main and auxiliary clock bus, and the outputs of element "AND" are connected to the inputs of the third element "OR."

Additional keywords: translation, USA, foreign technology

Figure 1 presents the functional diagram of the proposed device; Fig. 2 - the time diagrams for its operation.

The shift register consists of the main flip-flops 1, 2, 3 and auxiliary flip-flops 4, 5, 6. Respectively the main and auxiliary sequence of pulses are fed to the inputs of register 7, 8.

Similar (in the scheme being examined - single) outputs of the main and auxiliary flip-flops of the very same digit are connected to the inputs of the elements "EXCLUSIVE-OR" 9, 10, 11.

Flip-flops 1 and 4 are connected with element 9, flip-flops 2 and 5 - with element 10, and flip-flops 3 and 6 - with element 11.

The outputs of the main flip-flop of each digit and the auxiliary flip-flop of the following digit are connected with other elements "EXCLUSIVE-OR" 12, 13, 14.

In the case being examined the zero outputs of flip-flops 1 and 5 are connected with element 12, flip-flops 2 and 6 - with element 13, and so forth.

The outputs of elements (EXCLUSIVE-OR" 9, 10, and 11 are connected with the input of element "OR" 15, the outputs of elements 12, 13, 14 - with the input of element "OR" 16. The outputs of elements 15 and 16 are connected through elements "AND" 17 and 18 to the inputs of element "OR" 19. The second inputs of elements "AND" 17 and 18 are connected with the outputs of flip-flop 20, and its separate inputs are connected to the inputs of registers 7 and 8.

The recording of the numbers in the flip-flops is accomplished through coincident circuits 21-23 connected with the inputs of register 7 or 8.

The digital designations in Fig. 2 indicate that the corresponding diagram reflects the change in voltage on the output of the elements of the circuit in Fig. 1 designated with the same digit (for flip-flops - on one's output).

Initially, let us examine the case where there are no errors in the register (see Fig. 2a).

To be specific, let us assume that the number "101" (reading from the left) has been recorded in the main flip-flops of register 1, 2, 3. The pulse of the auxiliary sequence which arrives first at the input of register 7 accomplishes the recording in the auxiliary flip-flops of the numbers which are recorded in the main flip-flops of the preceding digits. Therefore, with the arrival of the auxiliary pulse "1" is recorded in flip-flop 5, and in flip-flop 6 - "0." The number from the main flip-flop of the preceding digit which is not shown in the drawing (for example "0") is recorded in flip-flop 4. Thus, with serviceable operation after the arrival of the auxiliary pulse each main flip-flop and auxiliary flip-flop of the next digit should be in the same state. In the example being examined flip-flops 1 and 5 are in state "1," and flip-flops 2 and 6 - in state "0." The elements which realize the logic operation "EXCLUSIVE-OR" are connected to the zero outputs of flip-flops 1, 5 and 2, 6.

The element "EXCLUSIVE-OR" provides a zero signal on the output only in the case where the signals on its input have the same value. Therefore, in this case the signals will have a zero value on the outputs of the elements "EXCLUSIVE-OR."

Consequently, the signal will also be zero on the output of the "OR" element 16.

The auxiliary pulse which reaches the input 7 is also fed to the one's input of flip-flop 20 and converts it to the one state. On the one output of this flip-flop the signal has a one value, and on the zero output - a zero value. These signals go to the inputs of the "AND" elements 17 and 18. Therefore, on the output of element 17 the signal will be zero, and the value of the signal on the output of element 18 will be determined by what signal there is on the output of the "OR" element 16. Since in this case this signal will be zero, zero signals go to the inputs of the "OR" element 19 and on its output the signal will also be zero, which shows the absence of errors in the register on the first (auxiliary) clock cycle.

Next the pulse of basic sequence goes to input 8. This pulse reaches the zero input of the flip-flop and converts it to the zero state. The flip-flop opens key 17 and closes key 18. Therefore the signal on the output of key 18 receives a zero value and the value of the signal on the output of the "AND" element 17 coincides with the signal arriving at it from element "OR" 15.

The main pulse which arrives at input 8 also accomplishes the recording, in the main flip-flops, of each digit of the numbers recorded by this point in time in the auxiliary flip-flops of the same digit. In the example being examined, flip-flop 2 finds itself in state "1" just as flip-flop 5, and flip-flop 3 - in state "0" just as flip-flop 6.

Since after the arrival of the main pulse the main and auxiliary flip-flops of the same digit should be in identical states with the register in good working order, the signals on the outputs of elements "EXCLUSIVE-OR" 9, 10, and 11 will have a zero value and the signal on the output of the "OR" element 15 will also be zero. This zero signal goes through the open element "AND" 17 to the input of element "OR" 19.

Consequently, on the output of element 19 the signal will have a zero value, which shows the absence of errors in the register on the second clock cycle.

Thus, in accordance with the given assumption, the push-pull shift register is supplied with two groups of logic elements "EXCLUSIVE-OR." One group (elements 12, 13, 14) is intended for monitoring the good working order of the register on the auxiliary clock cycle (i.e., on the time segment between the auxiliary and main pulses), and the second group (elements 9, 10, and 11) - for monitoring on the main clock cycle (on the time segment between the main and following auxiliary pulses).

The outputs of each group are combined using elements "OR" 16 and 15 and are connected for the time of the duration of the corresponding clock cycle to the outputs of the "OR" circuit 19 using

flip-flop 20. Therefore, if errors arise in the register in the process of transmitting information on one or another clock cycle, i.e., a mismatch appears between the corresponding flip-flops, this will be immediately recorded by the corresponding "EXCLUSIVE-OR" element.

Naturally, an error which arose on the corresponding clock cycle simultaneously in two flip-flops connected with one element "EXCLUSIVE-OR" will not be detected. However, the probability of such errors, as experiments show, is very small in comparison with the probability of single errors.

As an example, let us examine the case where with the same initial combination of states "101" a malfunction of flip-flop 5 occurs on the auxiliary clock cycle (see Fig. 2b). Here, instead of transferring to the one state as should be the case when in good working order, flip-flop 5 remains in the zero state.

Consequently, if the signals on the outputs of the "EXCLUSIVE-OR" element 12. are different, the output signal of this element will have a one value. The signal goes through element "OR" 16 and the "AND" circuit 18 open on the auxiliary clock cycle to the output of element "OR" 19, which shows errors in the register.

With a similar examination, one can be convinced that the errors in the register are also detected on the main clock cycle.

Subject of Invention

A push-pull shift register with the detection of errors which contains a main and auxiliary flip-flops in each bit, the outputs of which are connected with the corresponding coincidents circuits, and elements "AND," "OR," and "EXCLUSIVE-OR," which is distinguished by the fact that to increase the reliability of detection the first outputs of the main and auxiliary flip-flop of each bit are connected with the inputs of one "EXCLUSIVE-OR" element, the output of which is connected with the input of the first "OR" element, the second outputs of the main flip-flop of each bit and the auxiliary flip-flop of the

subsequent bit are connected with the inputs of the other "EXCLUSIVE-OR" element, the output of which is connected with the input of the second "OR" element, the outputs of the "OR" elements are connected with the input of the "AND" element which corresponds to it, the second input of which is connected with the output of the additional flip-flop, the outputs of which are connected with the main and auxiliary timing bus, and the outputs of the "AND" elements are connected to the inputs of the third "OR" element.

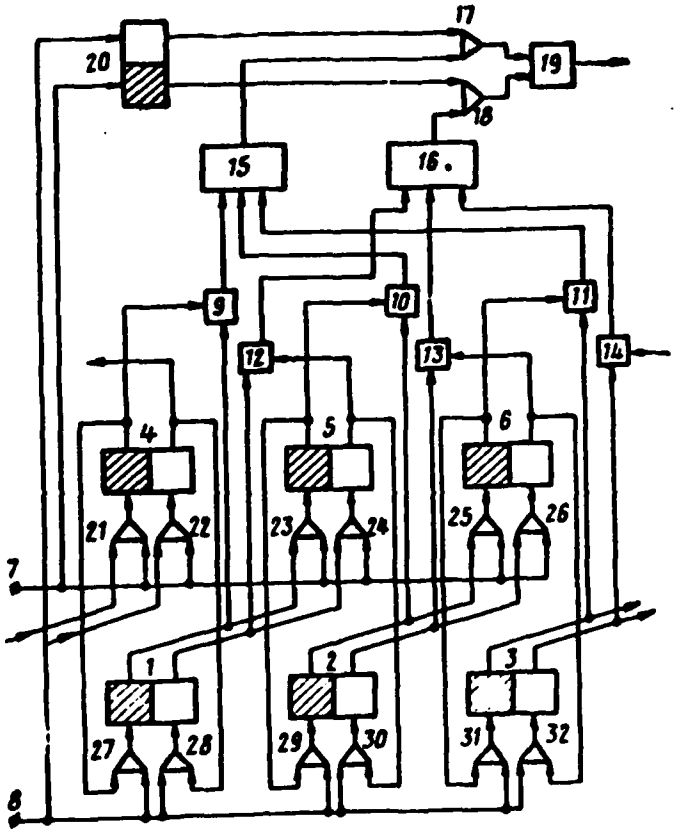


Fig. 1.

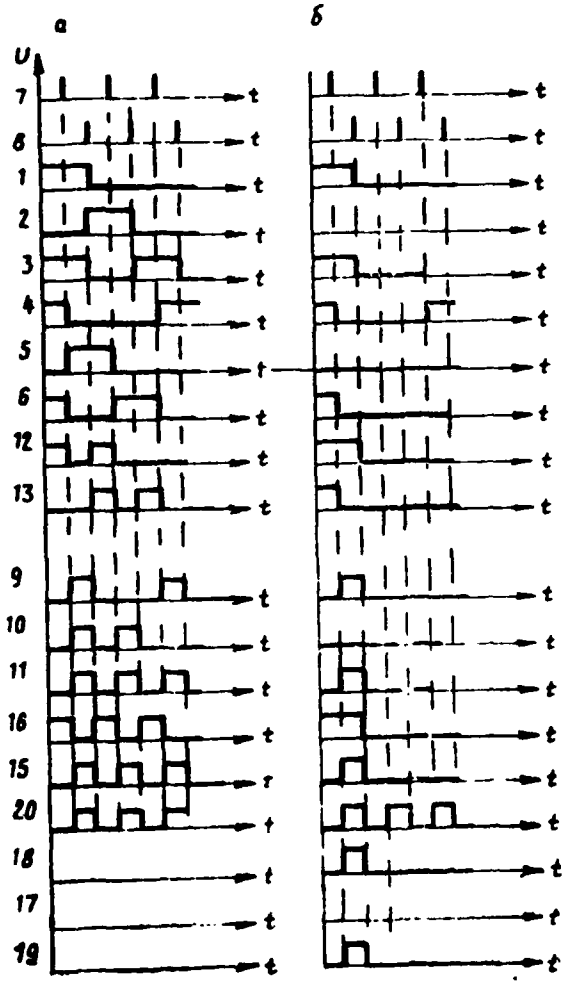


Fig. 2.

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